IN THE CLAIMS:

Claims 1-5 (Cancelled)

6. (Currently amended) A method of forming a dual damascene interconnect structure of an integrated circuit device, said interconnect structure having a low-k dielectric material deposited over an underlying metal layer, comprising the steps of:

a. forming a tri-part mask layer overlaying the low-k dielectric material, the mask layer including:

~~a.~~ i. ~~forming~~ a passivation mask film over the low-k dielectric material;

~~b.~~ ii. ~~forming~~ a non-metallic barrier mask film overlaying the passivation mask film; and

~~c.~~ iii. ~~forming~~ a metallic mask film overlaying the barrier mask film;~~, and said passivation barrier and metallic mask films forming a mask layer overlaying said low-k dielectric material;~~

~~d.~~ b. etching a trench within the mask layer, through at least the metallic mask film, without penetrating through the passivation layer ~~low-k dielectric material to a predetermined depth of the low-k dielectric material~~; and [[,]]

~~e.~~ c. after etching the trench in the mask layer, then etching a via through the mask layer within the trench and through the low-k dielectric material to the underlying metal layer before transferring the trench to the low-k dielectric

material..

7. (Original) The method of claim 6 wherein said passivation mask film comprises silicon dioxide or silicon ~~carbonite~~ carbide.

8. (Original) The method of claim ~~8~~ 6 wherein said barrier mask film comprises silicon nitride.

9. (Original) The method of claim ~~8~~ 6 wherein said metallic mask film comprises a refractory metal or a refractory metal alloy.

10. (Original) The method of claim 9 wherein said refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten, and said refractory metal alloy is chosen from the group of refractory metal alloys comprising titanium nitride and tantalum nitride.

11. (Original) The method of claim 6 further including the step of forming a photoresist layer over the metallic mask film, patterning a trench feature in the photoresist layer, etching a trench through the metal mask film and the barrier mask film to the passivation mask film.

12. (Original) The method of claim ~~6~~ 11 further including the step of forming a photoresist layer over the low-k dielectric material, and patterning a via feature in the photoresist layer.

13. (Currently amended) The method of forming an interconnect structure on an integrated circuit device having a low-k dielectric material deposited over an underlying metal layer, and a mask layer deposited on the low-k dielectric material, and said mask layer having a desired etch selectivity with respect to the low-k dielectric material, the method comprising the step of forming a non-metallic barrier layer interposed between a passivation layer and a metallic film ~~as part of the~~ to create a composite mask layer to increase the etch selectivity of the mask layer with respect to the low-k dielectric layer.

14. (Original) The method of claim 13 wherein said metallic film comprises a refractory metal or a refractory metal alloy.

15. (Original) The method of claim 14 wherein said refractory metal is chosen from the group of refractory metals including titanium, tantalum and tungsten and said refractory metal alloy is chosen from the group of refractory metal alloys including titanium nitride or tantalum nitride.

16. (Currently amended) The method of claim 13 further~~ing~~ including the steps of forming a passivation mask film over the dielectric material, forming a barrier mask film over the passivation mask film and said metallic film is formed over the barrier mask film.

17. (Original) The method of claim 15 wherein said passivation mask film comprises silicon dioxide or silicon carbonite.

18. (Original) The method of claim 15 wherein said barrier mask film comprises silicon nitride.

19. (Original) The method of claim 13 further including the steps of etching a trench within the low-k dielectric material to a predetermined depth of the low-k dielectric material, etching a via through the low-k dielectric material to the underlying metal layer of the low-k dielectric material, and depositing a conductive metal within the via and trench.

20. (Original) The method of claim 19 wherein the conductive metal is deposited on the integrated circuit chip outside of the via and the trench and the method further including the steps of planarizing the integrated circuit chip, and removing said excess conductive metal, the metallic mask layer and the barrier mask film.

21. (New) A method for the fabrication of a semiconductor device including a wafer substrate having a dielectric material formed over a metallization layer formed over said wafer substrate, comprising the steps of:

(a) forming a mask layer over the dielectric material wherein said mask layer includes a passivation film, and said mask layer having a known etch selectivity with respect to the dielectric material;

(b) forming a non-metallic barrier layer over the passivation film;

(c) depositing a metallic mask film over the barrier layer to increase the etch selectivity of the mask layer;

(d) patterning a first feature in the mask layer after depositing the metallic mask film;

(e) etching the first feature through the metallic mask film without exposing the underlying dielectric material after patterning the feature in the mask layer;

(f) patterning a second feature in the mask layer, said second feature overlapping at least a portion of the first feature;

(g) etching the second feature in the dielectric material in accordance with the patterned second feature in the mask layer before removing remaining portions of the passivation mask film and the metallic mask film;

(h) transferring the first feature from the mask layer to the underlying dielectric material after etching the second feature through the dielectric material to the metallization layer; and

(i) depositing a conductive metal in the first feature and in the second feature.

22. (New) The method of claim 21 wherein said etching step comprises the step of etching the feature in the mask layer through the metallic mask film and non-metallic barrier mask film down to the passivation mask film, then removing the metallic mask film and barrier mask film after etching the first and second features in the dielectric material, and before depositing the conductive metal in the feature.

23. (New) The method of claim 21 wherein said step of patterning includes patterning a first feature having a predetermined width different from a predetermined width of the first feature, and patterning a second feature having a predetermined width, said second feature being aligned with respect to said first feature.

24. (New) The method of claim 23 wherein said etching step includes etching the first feature in the mask layer through the metallic mask film and to the passivation mask film before patterning the second feature, and then

etching the second feature a predetermined depth in the dielectric material, before etching the first feature of the dielectric material to a predetermined depth of the dielectric material spaced above the predetermined depth of the second feature.